REMARKS/ARGUMENTS

An Office action was issued on January 2, 2009 in relation to the above referenced application. In the Office action, claims 1-6 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Pat. Publ. No. 2001/0018759 to Andreev et al. ("Andreev") in view of U.S. Pat. No. 5,742,510 to Rostoker et al. ("Rostoker"). Claims 1-6 are pending. Reconsideration and reexamination are respectfully requested. The Examiner is thanked for attention to the application.

Joint Ownership

The Office action states, "This application currently names joint inventors." (Office action, page 2). The Office action further reminds the applicant of its obligation under 35 CFR 1.56 to point out the inventor and invention dates of any claims that were not commonly owned at the time a later invention was made. Applicant wishes to point out, however, that this application has always listed only one inventor, Dr. Michael Thomas Greene. Further to this point, public pair indicates that an executed declaration was received at the U.S.P.T.O. on February 9, 2004 for the above referenced patent application. The executed declaration recites a single inventor, Dr. Michael Thomas Greene. Applicant submits that Dr. Greene is the sole inventor.

Claims Rejections - 35 U.S.C. § 103(a)

The Office action rejected claims 1-6 under 35 U.S.C. §103(a) as being unpatentable over Andreev in view of Rostoker.

Applicant disagrees with the above-mentioned obviousness rejection on the basis that the combination proposed in the rejection is not possible, would not have been considered by a worker in the art at the time the invention was made, and that even if such a combination were attempted, the presently claimed invention would not result.

The rejection states that "Andreev et al. clearly show and disclose, a method of determining the routing ... of interconnected regions ... of a routing problem by considering all required connections in parallel independently". Applicant respectfully submits that this statement is incorrect. Andreev does not consider all required connections in parallel independently; Andreev only considers all required connections substantially in parallel independently (or simultaneously), or in parallel independently (or simultaneously) where they do not overlap. Indeed, Andreev's abstract (which is relied upon by Examiner) states, "A method for ... routing nets ... with parallel processors operating **substantially** simultaneously." Applicant is frankly surprised and disappointed that the Examiner continues to assert that Andreev shows a method that considers all required connections in parallel independently, when it seemed during the telephone interview of September 19, 2008 that this distinction had been fully understood.

It is also noted that Rostoker describes a method of placement and routing of cells on a chip, and further describes how to implement this method in a highly parallelised way. These two strands are effectively separate: the placement and routing algorithms are put into a framework of parallelisation, but either the placement and routing algorithms themselves or the parallelisation framework could be used separately in a different context as part of a different algorithm. Neither of these strands embodies or relates to the algorithm of the pending claims.

It is pointed out that in Rostoker, the placement and routing is for <u>cells on a chip, not components on a printed circuit board (PCB)</u> as in the present application. In addition, the described routing is <u>channel routing, not gridless PCB routing</u>. Furthermore, the method described in Rostoker for distributing 'tasks' efficiently between multiple processors is not considered by the present application.

However, the rejection states that a worker skilled in the art who read Rostoker and Andreev would combine these to create the method claimed in the present application. Applicant considers that this is incorrect.

The Rostoker placement and routing algorithms are specific to the placement and routing of cells on an integrated circuit, whereas the routing algorithms in Andreev are concerned with

the routing of chips on a PCB. Presumably, therefore, the Examiner considers that the Andreev routing algorithms combined with the Rostoker parallelisation framework would yield an algorithm similar to that of the present invention. Although the Rostoker parallelisation would indeed be a sensible way to implement a parallelisation framework to support the separate routing tasks described in Andreev, this would still not make Andreev able to route the nets fully in parallel, independently and simultaneously. The combination of these algorithms would therefore not be similar to the algorithm of the present invention, where all nets can be routed fully in parallel, independently, and simultaneously.

In this regard, Applicant refers the Examiner to the arguments previously set forth in the response submitted November 11, 2007 in response to the Office action of September 21, 2007. That response clearly demonstrated that:

a)   Andreev is not able to route every net simultaneously;

b)   Andreev's algorithm cannot be made fully simultaneous by any modification obvious to someone skilled in the art; and

c)   In contrast, the method of the present invention routes all nets fully independently, simultaneously, and in parallel.

The Andreev routing algorithm cannot be adapted to be simultaneous. Applicant contends that a "reader knowledgeable in routing algorithms could not, using this algorithm as a basis, adapt it to route all nets in parallel". The basic operation of the algorithm requires occupancies and the corresponding penalties to be written to the edges in the graph representing the routable area, and these values cannot be accessed by more than one net at a time. Paragraph [0216] of Andreev states, "We need to make sure that while working in parallel we never need to adjust the same edge at the same time." This demonstrates that the Andreev routing algorithm cannot route all nets in parallel simultaneously, since any two affecting the same edge area must be routed serially. The paragraph goes on to say, "The easiest way to do that is to make sure that the nets worked on simultaneously are not in the same area," and outlines an approach to enforce this. That is, the approach in paragraphs [0217] and [0218] is not the only way of stopping edges from being accessed simultaneously; but some such mechanism is required.

The routing chosen is as cheap as possible given the penalties currently on edges it must cross. When a net is routed, the edge occupancies are updated (see paragraph [0206] of Andreev) to reflect the chosen route. This, of course, affects the routing choices of subsequent nets. So from the point of view of an individual edge, the nets that may cross it must be routed serially, because one net cannot be changing the edge's occupancy while another is trying to read it.

As an example, suppose two nets A and B are being routed simultaneously and two edges E0 and E1 have projected occupancy of 0.5 from both nets. E0 currently has a lower penalty than E1, but if either net is routed across E0, E0 will then have a higher penalty than E1. If A is routed first, A will bag the cheaper E0, and B will be left to go across E1. If B is routed first, B will bag the cheaper E0, and A will only be left the more expensive E1. But if they are routed simultaneously, A and B may both read the penalty values at the same time, may both decide to cross E0, and will both grab the first edge, which may in fact not be wide enough to accommodate both routes at once, leading to invalid routing.

This simple example shows that Andreev is fundamentally non-symmetric and non-simultaneous (even though it is stated to be 'substantially simultaneous').

Based on the foregoing, applicant strenuously urges that the method of applicant's claims 1-6 would not be obvious to a worker skilled in the art who considered the Andreev and Rostoker references. The proposed combination would not be obvious and, even if attempted, would not yield the claim method. Therefore, applicant submits that the rejection is improper and should be withdrawn. Prompt allowance of the claims is therefore requested.
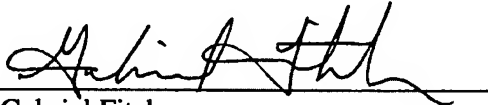
If in considering this response it appears that a discussion with applicant's attorney would be helpful in resolving any remaining issues in this application, the Examiner is invited to telephone the undersigned attorney for applicant at the number indicated.

Respectfully submitted,

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